Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (original) A method of fabricating a silicon mirror device comprising:

providing a p-doped single crystal silicon substrate wafer having a frontside and a backside;

forming first and second n-doped regions at a surface of said substrate wherein said first n-doped regions have a first thickness and said second n-doped regions have a second thickness larger than said first thickness;

forming a hard mask on said backside of said wafer;

depositing a silicon oxide layer on said frontside of said wafer;

depositing an aluminum layer on said silicon oxide layer and patterning said aluminum layer to leave aluminum on said silicon oxide layer overlying some of said second n-doped regions to form thermal actuators;

depositing a dielectric layer overlying said patterned aluminum layer and said silicon oxide layer and patterning said dielectric layer to form a mask for flexible springs over portions of said first n-doped regions;

depositing and patterning a metal layer overlying said dielectric layer to form bond pads to said thermal actuators contacting said patterned aluminum layer through openings in

said dielectric layer and to form reflecting mirror surfaces overlying others of said second n-doped regions not covered by said patterned aluminum layer to form micromirrors;

thereafter etching away said substrate from said backside of said wafer stopping at said first and second n-doped regions;

thereafter dicing said wafer into mirror array chips;

thereafter etching away said dielectric layer from said frontside of said wafer to expose portions of said first n-doped regions; and

etching away from said frontside said exposed first n-doped regions not covered by said mask to form flexible springs in said first n-doped regions wherein said second n-doped regions covered by said patterned aluminum layer form thermal actuators and said wherein said flexible springs connect said micromirrors to said thermal actuators.

2. (original) The method according to Claim 1 wherein said forming said first and second n-doped regions comprises:

implanting first phosphorus ions through a mask into said substrate to a first depth; and

implanting second phosphorus ions globally into said substrate to a second depth shallower than said first depth wherein said first depth is increased to a third depth wherein said phosphorus ions diffused to said second depth form said first n-doped regions and wherein said phosphorus ions diffused to said third depth form said second n-doped regions.

3. (original) The method according to Claim 1 wherein said forming said first and second n-doped regions comprises:

growing an epitaxial silicon layer on said p-doped silicon substrate; and

patterning said epitaxial silicon layer to form said first n-doped regions and said second n-doped regions.

4. (original) The method according to Claim 3 wherein said patterning is performed using a deep reactive ion etching (DRIE) process.

5. (original) The method according to Claim 1 wherein said forming said hard mask comprises:

depositing a first nitride layer on said substrate on said backside of said wafer;

depositing a TEOS oxide layer overlying said first nitride layer; and

depositing a second nitride layer overlying said TEOS oxide layer to form said hard mask.

6. (original) The method according to Claim 5 wherein said first nitride layer is deposited to a thickness of between about 1200 and 1800 Angstroms, said TEOS oxide layer is deposited by plasma enhanced chemical vapor deposition (PECVD) to a thickness of between about 800 and 1200 Angstroms, and said second nitride layer is deposited by PECVD to a thickness of between about 1500 and 2500 Angstroms.

7. (original) The method according to Claim 1 wherein said aluminum layer is deposited to a thickness of about 1 micron.

8. (original) The method according to Claim 1 wherein said depositing said metal layer comprises:

depositing a chromium layer to a thickness of between about 100 and 200 Angstroms; and

depositing a gold layer overlying said chromium layer to a thickness of between about 400 and 600 Angstroms.

9. (original) The method according to Claim 1 wherein said etching away said substrate from said backside of said wafer comprises electrochemical etching in aqueous KOH.

10. (original) The method according to Claim 1 wherein said etching away said substrate from said backside of said wafer comprises a combination of DRIE and electrochemical etching in aqueous KOH.

11. (original) The method according to Claim 1 wherein said etching away said dielectric layer from said top side of said wafer comprises DRIE.

12. (original) The method according to Claim 1 wherein said etching away said dielectric layer from said top side of said wafer separates said thermal actuators, said flexible springs, and said micromirrors simultaneously.

13. (original) The method according to Claim 1 wherein edges of said micromirrors are thinner than central portions of said micromirrors.

14. (original) A method of fabricating a silicon mirror device comprising:

providing a p-doped single crystal silicon substrate wafer having a frontside and a backside;

forming first and second n-doped regions at a surface of said substrate wherein said first n-doped regions have a first thickness and said second n-doped regions have a second thickness larger than said first thickness;

forming a hard mask on said backside of said wafer;

depositing a silicon oxide layer on said frontside of said wafer;

depositing an aluminum layer on said silicon oxide layer and patterning said aluminum layer to leave aluminum on said silicon oxide layer overlying some of said second n-doped regions to form thermal actuators;

depositing a dielectric layer overlying said patterned aluminum layer and said silicon oxide layer and patterning said dielectric layer to form a mask for flexible springs over portions of said first n-doped regions;

depositing and patterning a metal layer overlying said dielectric layer to form bond pads to said thermal actuators contacting said patterned aluminum layer through openings in said dielectric layer and to form reflecting mirror surfaces overlying others of said second n-doped regions not covered by said patterned aluminum layer to form micromirrors;

thereafter etching away said substrate from said backside of said wafer stopping at said first and second n-doped regions;

thereafter dicing said wafer into mirror array chips;

thereafter etching away said dielectric layer from said frontside of said wafer to expose portions of said first n-doped regions; and

etching away from said frontside said exposed first n-doped regions not covered by said oxide mask to form flexible springs in said first n-doped regions wherein said second n-doped regions covered by said patterned aluminum layer form thermal actuators and wherein said flexible springs connect said micromirrors to said thermal actuators and wherein each mirror element in each of said mirror array chips comprises one micromirror and four thermal actuators.

15. (original) The method according to Claim 14 wherein said forming said first and second n-doped regions comprises:

implanting first phosphorus ions through a mask into said substrate to a first depth; and

implanting second phosphorus ions globally into said substrate to a second depth shallower than said first depth wherein said first depth is increased to a third depth wherein said phosphorus ions diffused to said second depth form said first n-doped regions and wherein said phosphorus ions diffused to said third depth form said second n-doped regions.

16. (original) The method according to Claim 14 wherein said forming said first and second n-doped regions comprises:

growing an epitaxial silicon layer on said p-doped silicon substrate; and

patterning said epitaxial silicon layer to form said first n-doped regions and said second n-doped regions.

17. (original) The method according to Claim 16 wherein said patterning is performed using a deep reactive ion etching (DRIE) process.

18. (original) The method according to Claim 14 wherein said forming said hard mask comprises:

depositing a first nitride layer on said substrate on said backside of said wafer;

depositing a TEOS oxide layer overlying said first nitride layer; and

depositing a second nitride layer overlying said TEOS oxide layer to form said hard mask.

19. (original) The method according to Claim 18 wherein said first nitride layer is deposited to a thickness of between about 1200 and 1800 Angstroms, said TEOS oxide layer is deposited by plasma enhanced chemical vapor deposition (PECVD) to a thickness of between about 800 and 1200 Angstroms, and said second nitride layer is deposited by PECVD to a thickness of between about 1500 and 2500 Angstroms.

20. (original) The method according to Claim 14 wherein said aluminum layer is deposited to a thickness of about 1 micron.

21. (original) The method according to Claim 14 wherein said depositing said metal layer comprises:

depositing a chromium layer to a thickness of between about 100 and 200 Angstroms; and

depositing a gold layer overlying said chromium layer to a thickness of between about 400 and 600 Angstroms.

22. (original) The method according to Claim 14 wherein said etching away said substrate from said backside of said wafer comprises electrochemical etching in aqueous KOH.

23. (original) The method according to Claim 14 wherein said etching away said substrate from said backside of said wafer comprises a combination of DRIE and electrochemical etching in aqueous KOH.

24. (original) The method according to Claim 14 wherein said etching away said dielectric layer from said top side of said wafer comprises DRIE.

25. (original) The method according to Claim 14 wherein said etching away said dielectric layer from said top side of said wafer separates said thermal actuators, said flexible springs, and said micromirrors simultaneously.

26. (original) The method according to Claim 14 wherein edges of said micromirrors are thinner than central portions of said micromirrors.

27-37. (canceled)